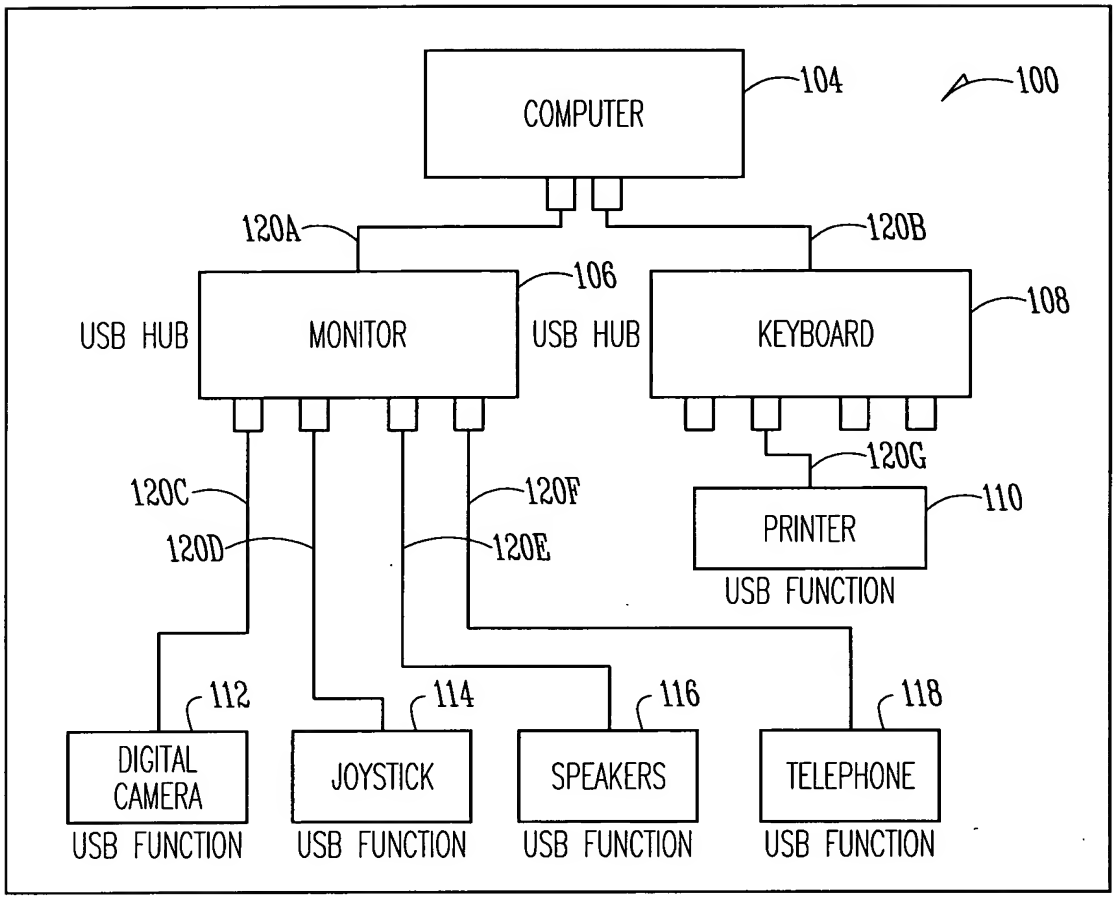
COMPUTER
104
100
120A
120B
106
USB HUB
MONITOR
USB HUB
KEYBOARD
108
120G
120C
120F
120D
120E
PRINTER
110
USB FUNCTION
112
114
116
118
DIGITAL CAMERA
JOYSTICK
SPEAKERS
TELEPHONE
USB FUNCTION
USB FUNCTION
USB FUNCTION
USB FUNCTION

Fig. 1

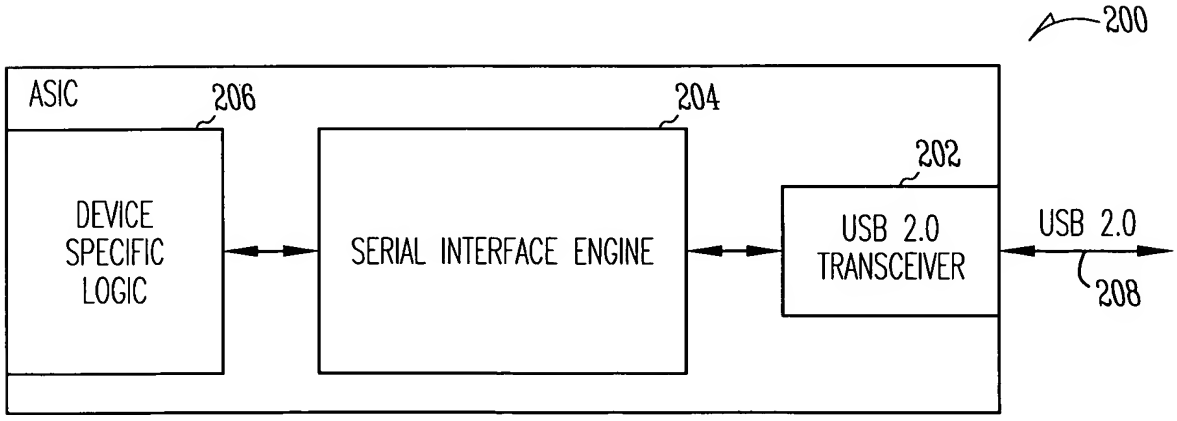
200
ASIC
206
204
202
DEVICE SPECIFIC LOGIC
SERIAL INTERFACE ENGINE
USB 2.0 TRANSCEIVER
USB 2.0
208

Fig. 2

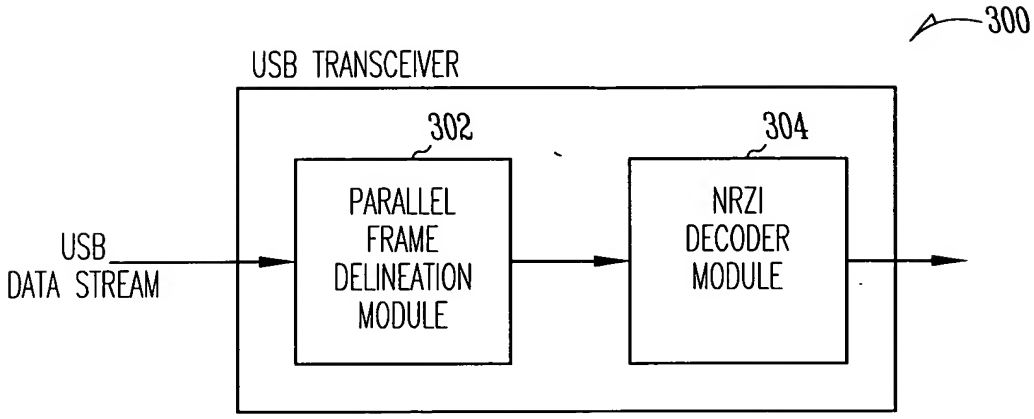

Fig. 3

10043848 - 100501

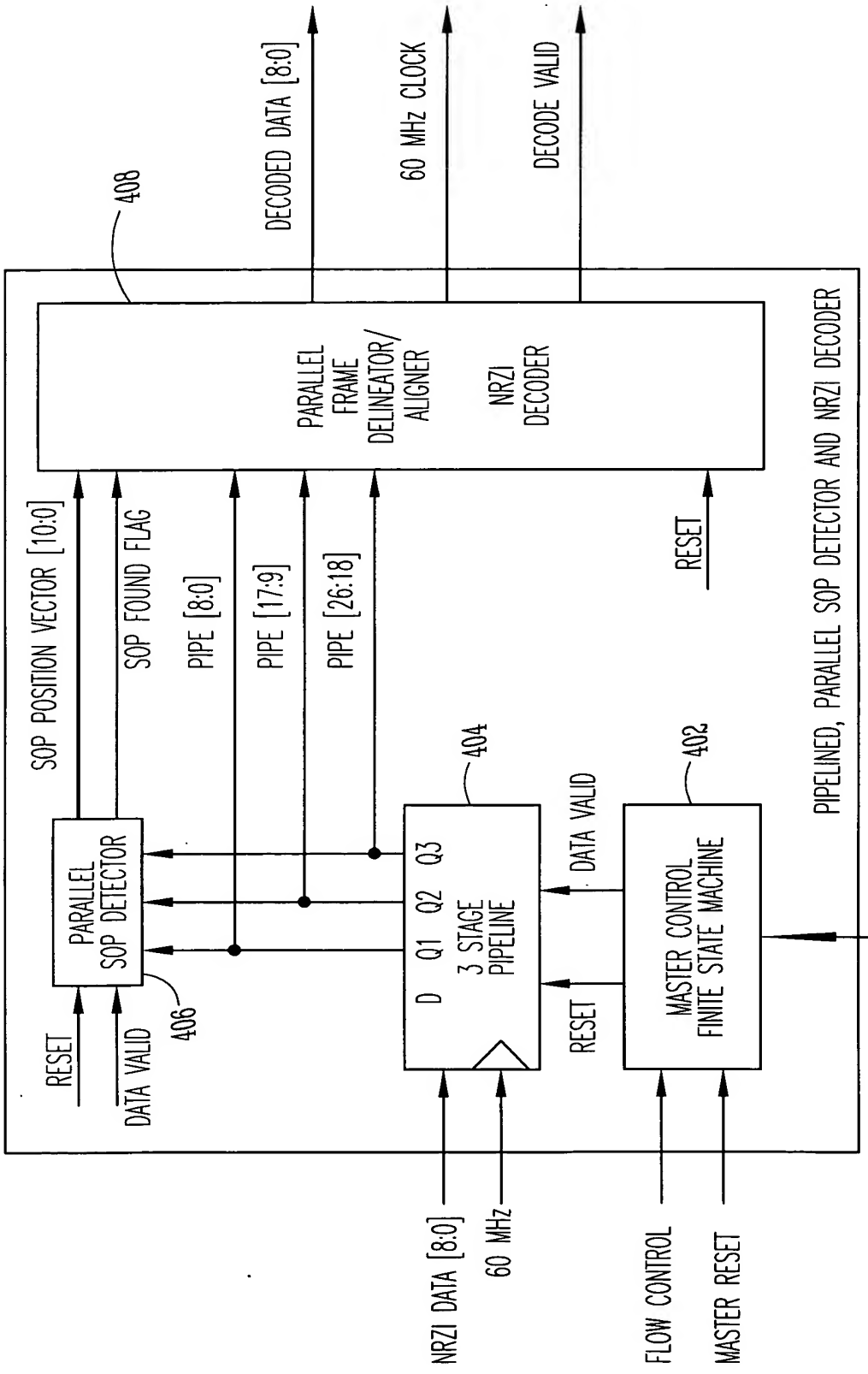
400
408
DECODED DATA [8:0]
60 MHz CLOCK
DECODE VALID
PARALLEL FRAME DELINEATOR/ ALIGNER
NRZI DECODER
SOP POSITION VECTOR [10:0]
SOP FOUND FLAG
PIPE [8:0]
PIPE [17:9]
PIPE [26:18]
RESET
PARALLEL SOP DETECTOR
406
404
D Q1 Q2 Q3
3 STAGE PIPELINE
DATA VALID
402
MASTER CONTROL FINITE STATE MACHINE
PIPELINED, PARALLEL SOP DETECTOR AND NRZI DECODER
EOP (END OF PACKET)
RESET
DATA VALID
NRZI DATA [8:0]
60 MHz
FLOW CONTROL
MASTER RESET

Fig. 4

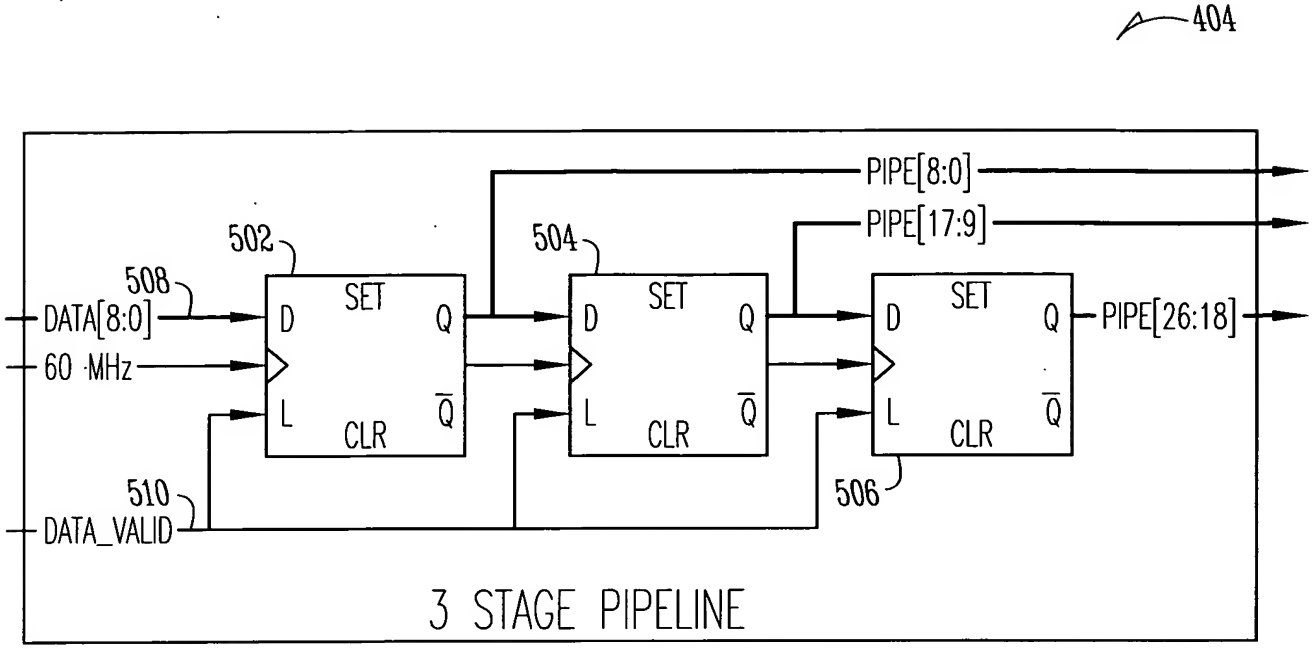
404
PIPE[8:0]
PIPE[17:9]
502
504
508
DATA[8:0]
60 MHz
SET
D
Q
L
CLR
Q̄
PIPE[26:18]
510
DATA_VALID
506
3 STAGE PIPELINE

Fig. 5

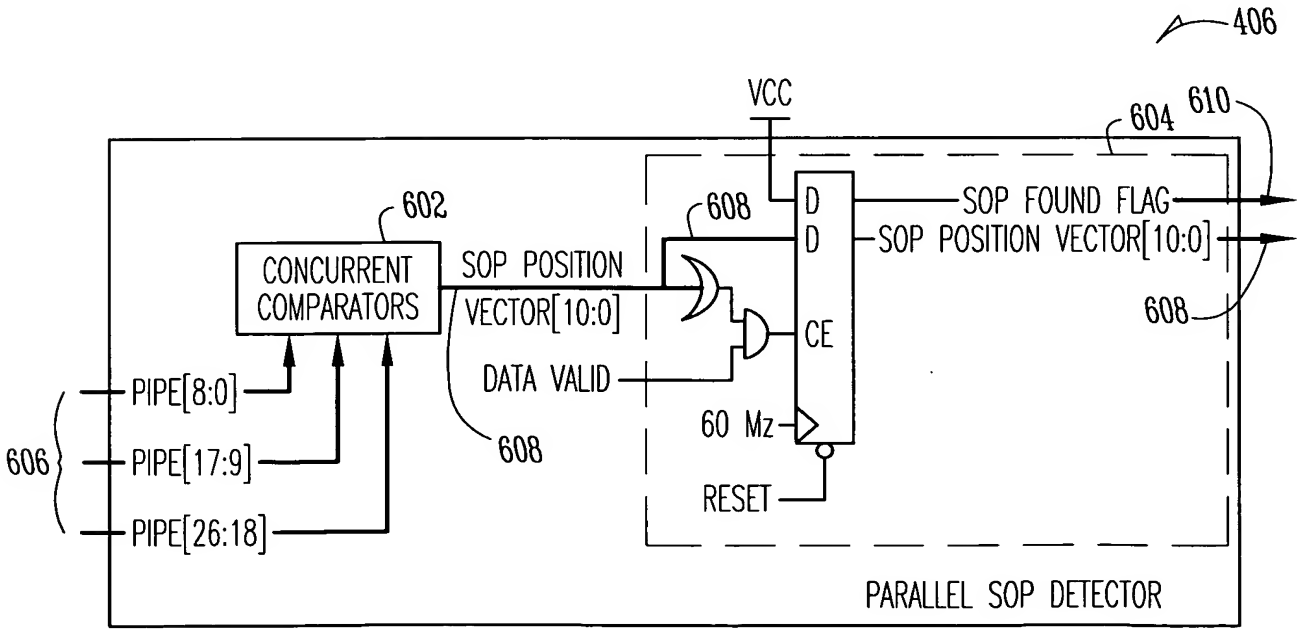
406
VCC
604
610
602
608
CONCURRENT COMPARATORS
SOP POSITION VECTOR[10:0]
D
SOP FOUND FLAG
SOP POSITION VECTOR[10:0]
CE
DATA VALID
60 Mz
RESET
606
PIPE[8:0]
PIPE[17:9]
PIPE[26:18]
PARALLEL SOP DETECTOR

Fig. 6

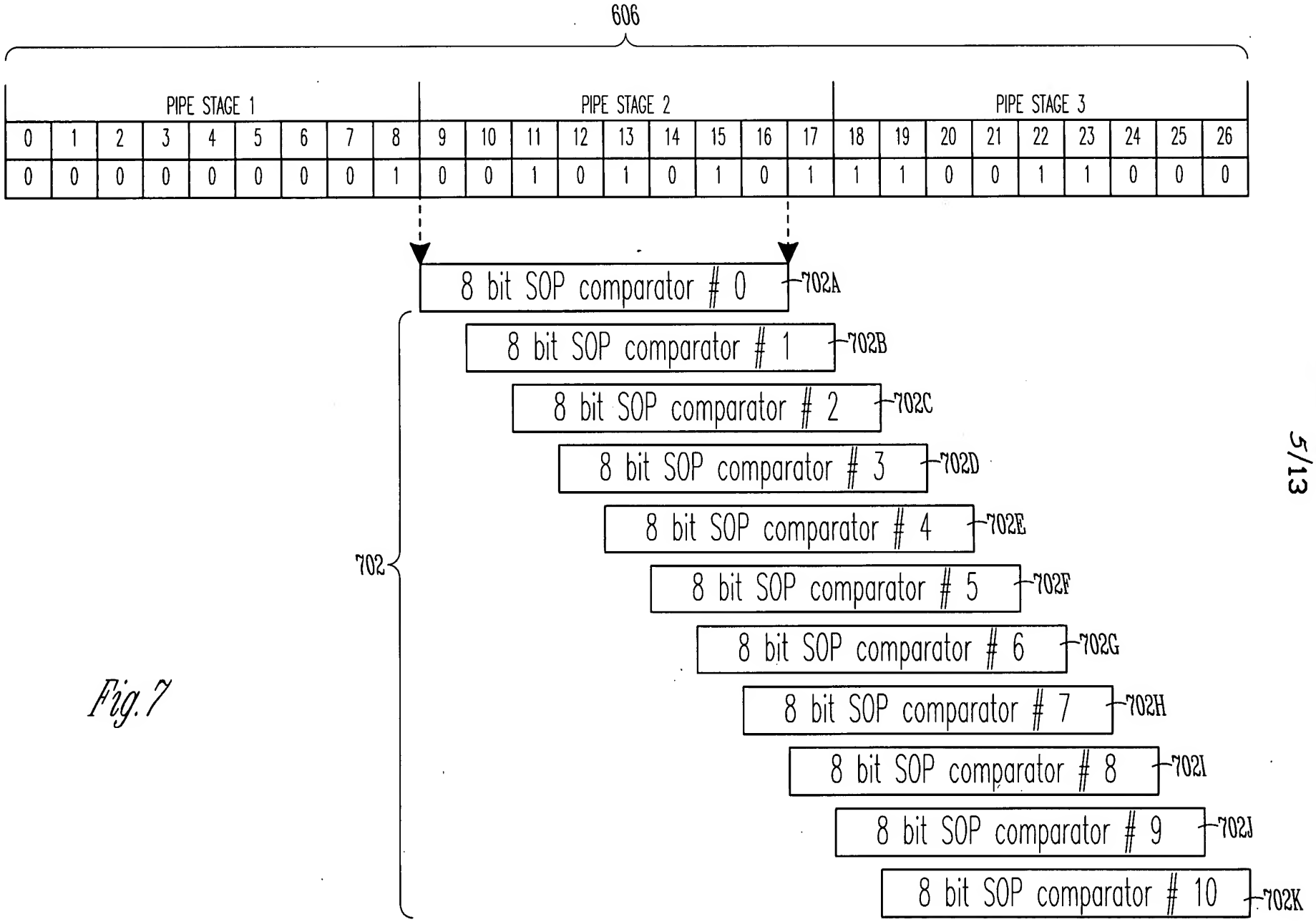
606
PIPE STAGE 1
PIPE STAGE 2
PIPE STAGE 3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 1 1 1 0 0 1 1 0 0 0
8 bit SOP comparator # 0 702A
8 bit SOP comparator # 1 702B
8 bit SOP comparator # 2 702C
8 bit SOP comparator # 3 702D
8 bit SOP comparator # 4 702E
8 bit SOP comparator # 5 702F
8 bit SOP comparator # 6 702G
8 bit SOP comparator # 7 702H
8 bit SOP comparator # 8 702I
8 bit SOP comparator # 9 702J
8 bit SOP comparator # 10 702K
702

Fig. 7

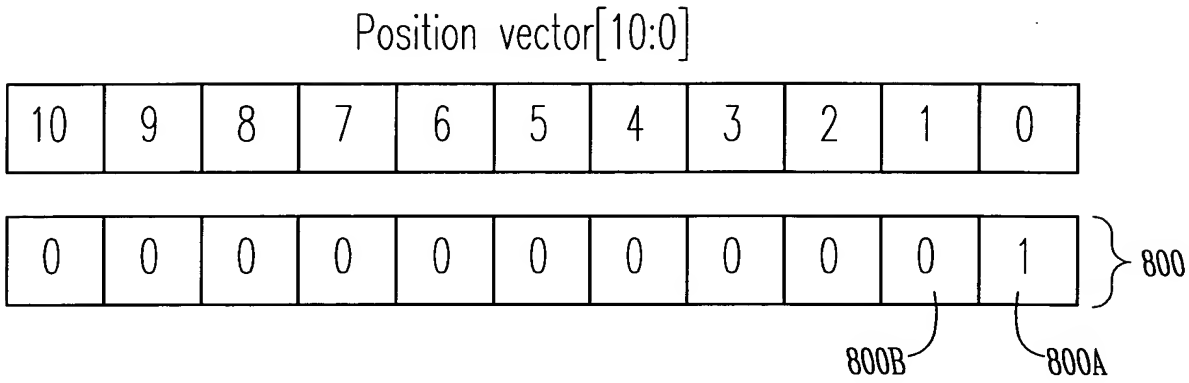
Position vector[10:0]
10
9
8
7
6
5
4
3
2
1
0
0
0
0
0
0
0
0
0
0
0
1
800
800B
800A

Fig. 8

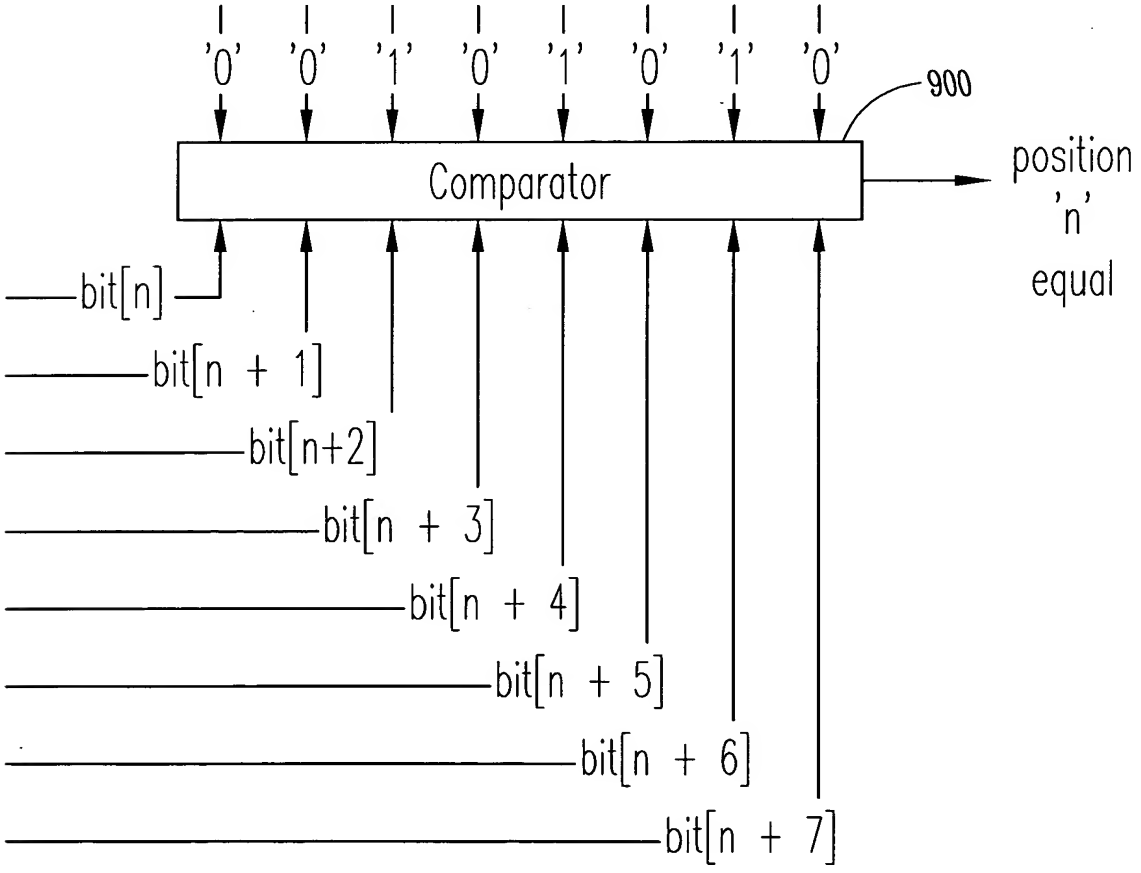
'0'
'0'
'1'
'0'
'1'
'0'
'1'
'0'
900
Comparator
position 'n' equal
bit[n]
bit[n + 1]
bit[n+2]
bit[n + 3]
bit[n + 4]
bit[n + 5]
bit[n + 6]
bit[n + 7]

Fig. 9

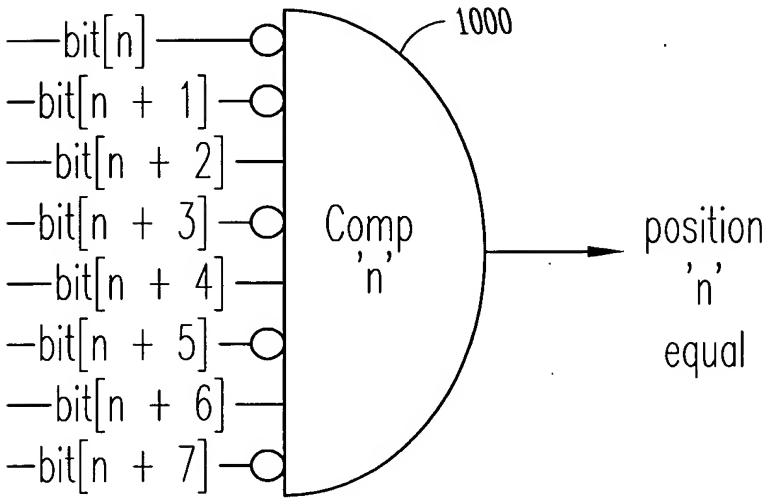

Fig. 10

Attorney Docket No. 884.311US1

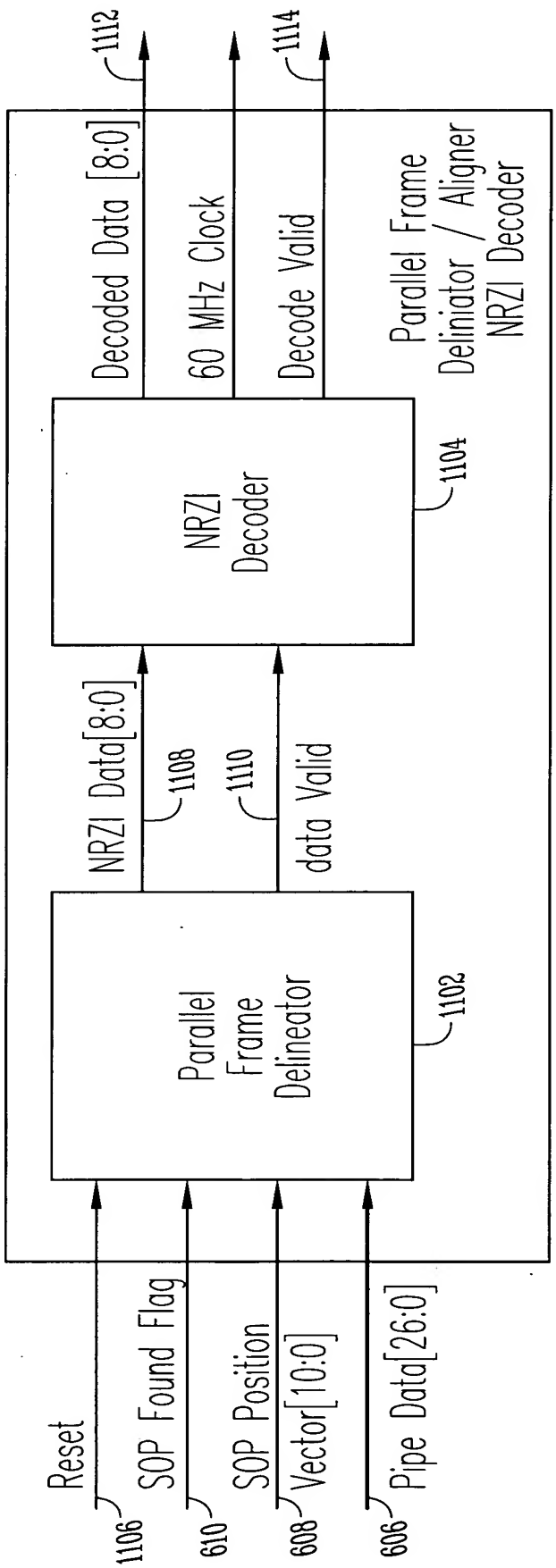

Fig. 11

"Express Mail" Label No. EV 339 744 907 US

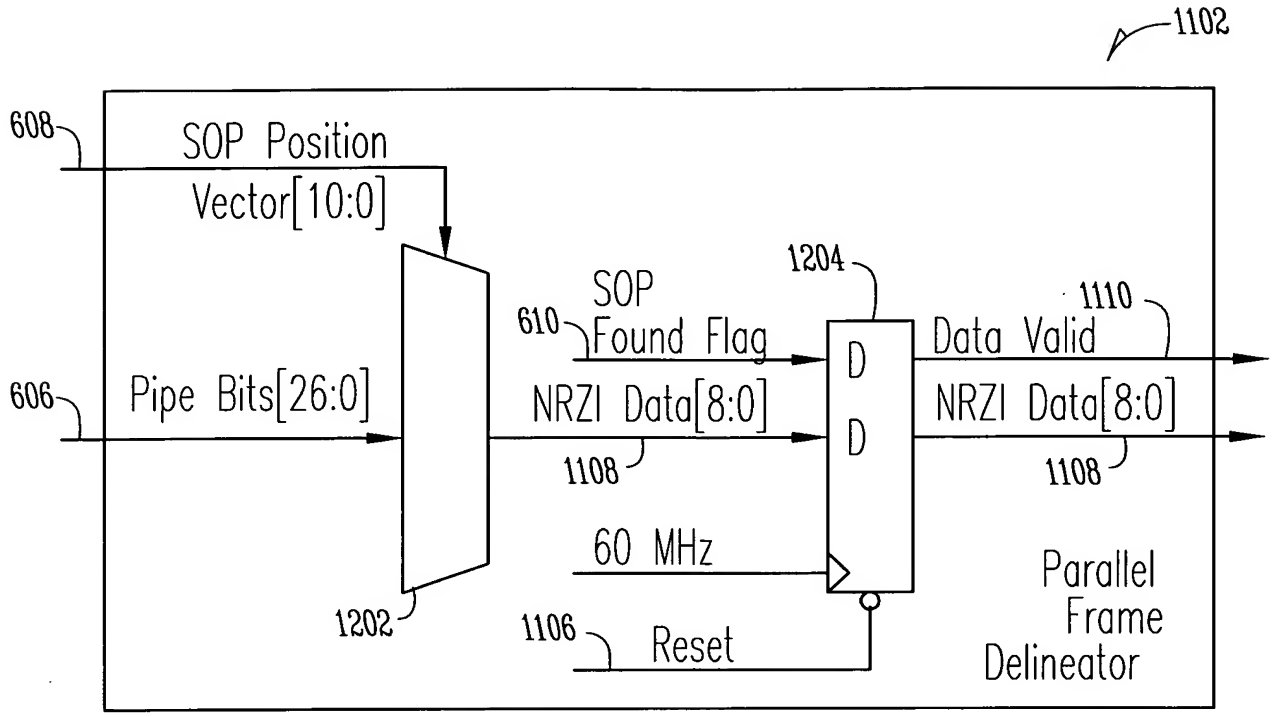

Fig. 12

Attorney Docket No.: 884.311US1

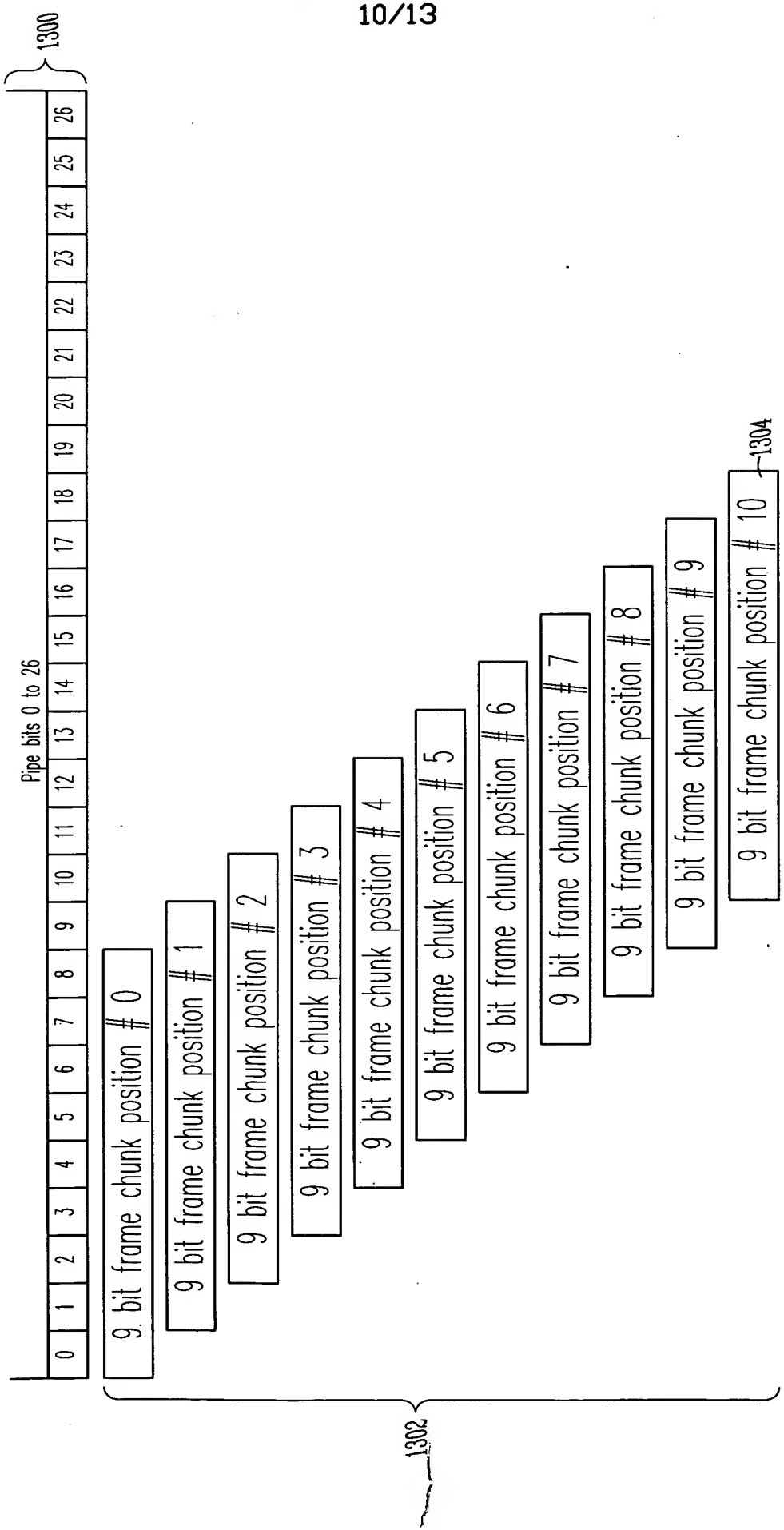
1300
Pipe bits 0 to 26
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
9 bit frame chunk position # 0
9 bit frame chunk position # 1
9 bit frame chunk position # 2
9 bit frame chunk position # 3
9 bit frame chunk position # 4
9 bit frame chunk position # 5
9 bit frame chunk position # 6
9 bit frame chunk position # 7
9 bit frame chunk position # 8
9 bit frame chunk position # 9
9 bit frame chunk position # 10
1304
1302

Fig. 13

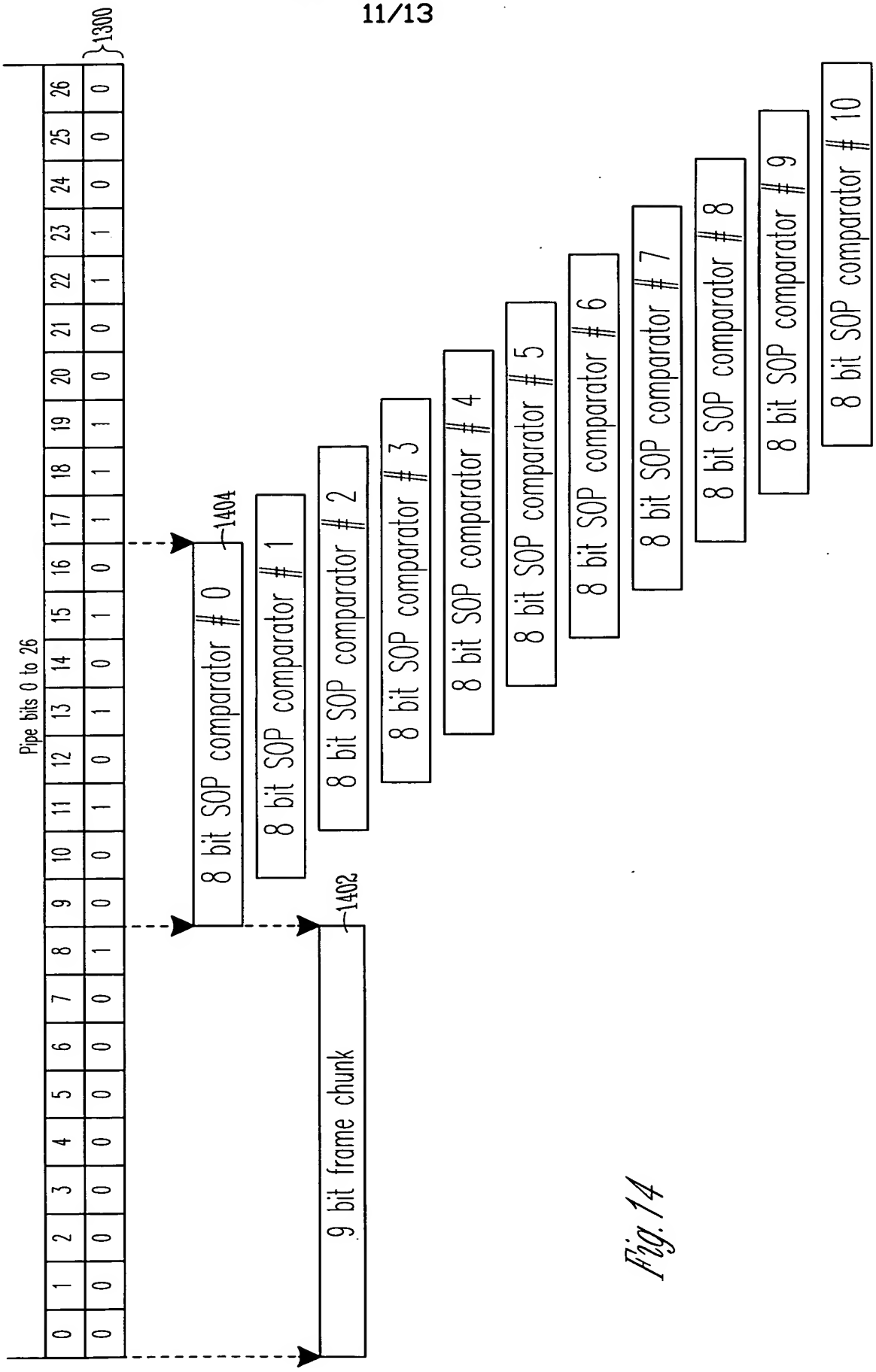
1300
Pipe bits 0 to 26
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 1 1 1 0 0 1 1 0 0 0
1404
1402
8 bit SOP comparator # 0
8 bit SOP comparator # 1
8 bit SOP comparator # 2
8 bit SOP comparator # 3
8 bit SOP comparator # 4
8 bit SOP comparator # 5
8 bit SOP comparator # 6
8 bit SOP comparator # 7
8 bit SOP comparator # 8
8 bit SOP comparator # 9
8 bit SOP comparator # 10
9 bit frame chunk

Fig. 14

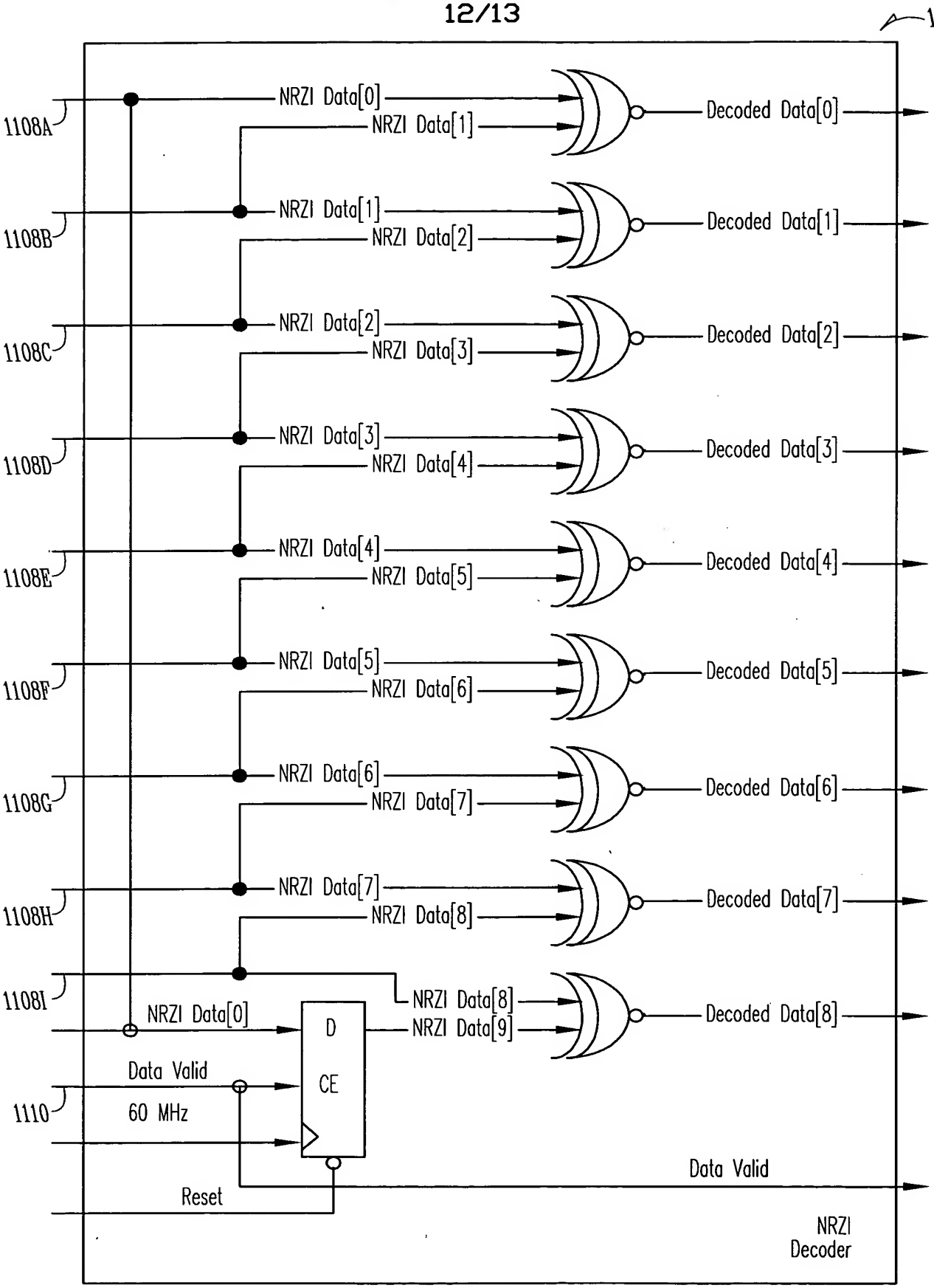
1104
1108A
1108B
1108C
1108D
1108E
1108F
1108G
1108H
1108I
1110
NRZI Data[0]
NRZI Data[1]
NRZI Data[2]
NRZI Data[3]
NRZI Data[4]
NRZI Data[5]
NRZI Data[6]
NRZI Data[7]
NRZI Data[8]
NRZI Data[9]
Decoded Data[0]
Decoded Data[1]
Decoded Data[2]
Decoded Data[3]
Decoded Data[4]
Decoded Data[5]
Decoded Data[6]
Decoded Data[7]
Decoded Data[8]
D
CE
Data Valid
60 MHz
Reset
Data Valid
NRZI Decoder

Fig. 15

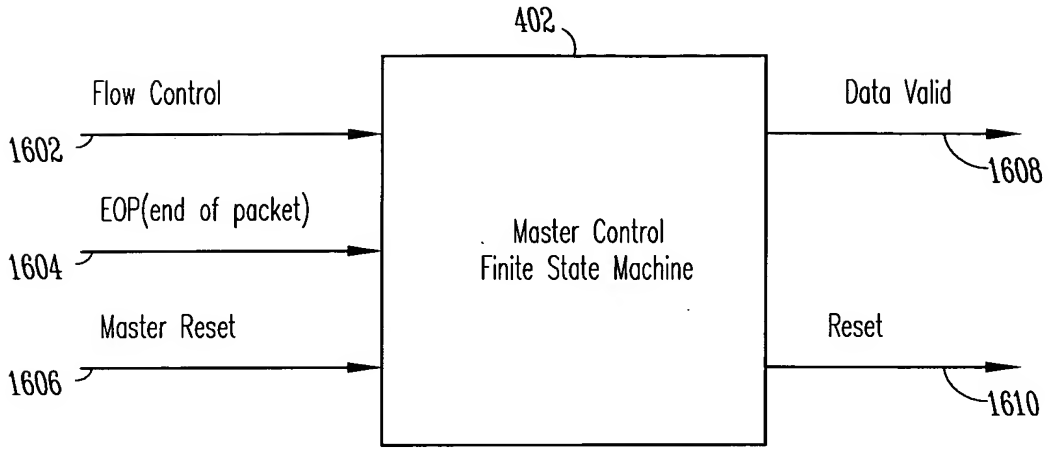
402
Flow Control
1602
EOP(end of packet)
1604
Master Reset
1606
Master Control
Finite State Machine
Data Valid
1608
Reset
1610

Fig. 16

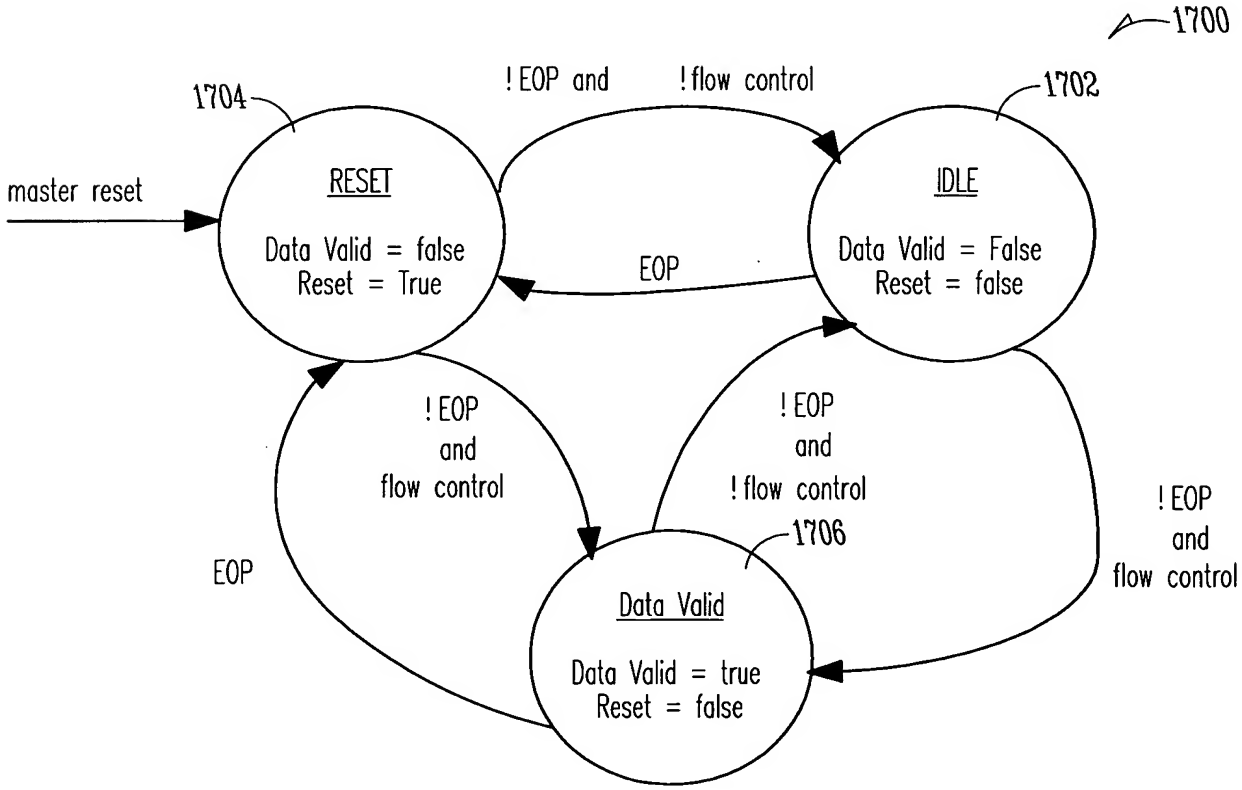
1700
1704
1702
! EOP and ! flow control
master reset
RESET
Data Valid = false
Reset = True
IDLE
Data Valid = False
Reset = false
EOP
! EOP and flow control
! EOP and ! flow control
EOP
1706
! EOP and flow control
Data Valid
Data Valid = true
Reset = false

Fig. 17